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WSN Low energy Optimization Technique Study

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Abstract (10pt)

Sensor networks are mostly distributed over a large area which may sometimes be harsh and uneven. Therefor the system must be tolerant to faults raised by the environment and also other intermittent problems. The sensed values must be very accurate and reliable. Various online and offline methods are used for validation. ATE is a hardware test used to test the readings. But ATE capabilities can't match the test requirements in terms of volume and speed. BIST is a test embedded within the system itself. But it has certain disadvantages like hardware and area overhead and also elevated power dissipation. Therefore SBST plays an important role in testing the sensor node. The SBST routines are used for this purpose. They can either be downloaded to the nodes or they may be available in the flash memory also. Various optimization methodologies have been discussed in the paper.

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1. Introduction

A Wireless Sensor Network is made up of a number of wireless sensor nodes that are dispersed around a geographical area. It can have a small number of nodes or a large number of nodes. They are obligated to quantify variables such as temperature, strain, and sound, among others. It has a wide range of uses in military applications, surveillance, and other areas.

The main features of a WSN are:

- Communication failures
- Heterogeneity of nodes
- Scalability to large scale of deployment
- Ability to withstand harsh environmental conditions
- Power consumption constrains for nodes using batteries or energy harvesting
- Ability to cope with node failures
- Mobility of nodes

A sensor network consists of a base station or a Sink. All data acquisition nodes are assigned on an individual basis, and then they are sent to the base station. Base station appropriately processes the data and obtains thecorresponding results. The nodes come together and form a network topology. If one of the nodes fails, all of the other nodes will reorganize to form a new topology.

One of the major limitations of the sensor is capacity. Therefore, each node should try to optimize the capacity to increase the life of the system. The basic architecture of a wireless sensor node consists of layers of different physical layers, data link layer, network layer , transport layer, application layer.

The paper deals with various optimization methodologies to optimize the power consumption and also the accuracy of the sensed readings and values by a sensor node.[1]

2. Existing Methodologies.

2.1 AUTOMATIC TEST EQUIPMENT (ATE)

ATE is one amongst the ways for testing the electronic circuits. It is termed as external methodology. The circuit-under-test is either the complete chip or simply a part of the chip. For the aim of testing, there ought to be inputs and process of the inputs it ought to manufacture outputs. The input is termed as input check vectors.They are binary patterns which might be applied to the CUTand the associated output responses ar the values observed on the outputs of the CUT. Then the output responses well-versed a comparator wherever they're compared against the expected responses.[2][3]. If all the output responses match the corresponding expected responses, then the system is marked as fault-free.Because the technology advances and the CUT grow additional advanced, the Ate capabilities can't match the check necessities in terms of volume and speedThe limitations of ATE paved way for Built-In-Self-Test (BIST).

2.2 BUILT-IN-SELF-TEST (BIST)

The main testing method incorporated is the hardware based test is termed as Built-In-Self-Test (BIST). BIST is the embedded hardware tester.Self testing is a significant strategy as the remote sensor framework or some other advanced framework might be defrauded to different flaws like primary, ecological, and so on Accordingly, it is vital that the framework is tested and analyzed and tested frequently during the lifetime of the framework.There are principally two kinds of BIST procedure.[4] They are on the online and Offline techniques. Flaws can be characterized as physical or logical imperfections in either the plan or execution of a specific gadget.Faults can be defined as physical or logical defects in either the design or implementation of a particular device. Faults when unreciginised may further lead to errors in system resulting in incorrect states. Errors may induce failures. Under a failure situation, the behaviour of the system will ne abnormal leading to hazard. Faults can be categorized into three: Design, Fabrication, and Operational. Design faults are those faults in the system's hardware.[5]

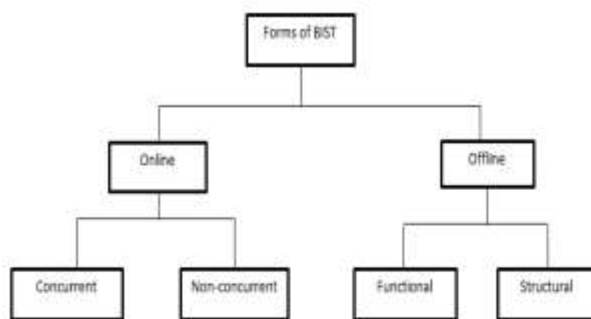

Figure 1: Forms of BIST

2.2.1 Online testing

The testing done during normal operation is called Online Testing. It will find the normal faults in the system by diagonising the error and if diagonised with eeror it will take necessary measures for corretingit.Online Testing can be further divided to Concurrent testing and Non concurrent Testing.

a) Non-Concurrent Testing:
   This testing is triggred by event or time.During the operation of the system, changes can happen to state of the system or key events may occur. This triggers non-concurrent testing which detects permanent faults.Non concurrent testing is dile during normal working of system.

b) Concurrent testing:
   The concurrent testing works simultaneously with the other normal operations of the system.Concurrent testing identifies the drawbacks as it can diagnose such faults during the operational life cycle of the system.

2.2.2 Offline Testing

Offline Testing is done when the system is Suspended. It can be classified in to Structrualand Functional

a) Structural
   Testing based on circuit under Test[CUT]
b) Functional
   Testing based in Structure of CUT.

2.3 BIST Architecture:

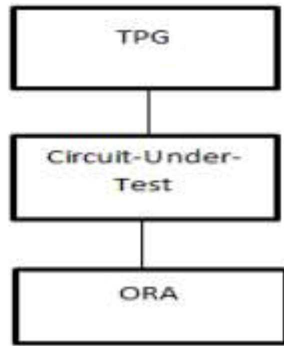

Figure 2:BIST Architecture.

Advantages of BIST:

- It has a hiererchial structure.
- BIST is cheap solution.
- No need of expensive ATE.
- Support concurrent Testing.
- Can be used for delay testing.
- Fast and Efficent

Disadvantages of BIST:

- Additional BIST Hardware
- Area Overload.
- Elevated power dissipation.

3.The Current Methodoldogy:

In SBST Software Based Self Testing the exection of a program takes palce in embedded processor.Here the structural faults can be identified during the functional internal resources.ISA and resourcse are made use by SBST. The self-test program is initially downloaded into the internal instruction memory and then to a low-cost external equipment. Then, it is executed by the microprocessor and then computes and stores self-test responses in the data memory. Finally, the external equipment brings back those self-test responses for evaluation.Thus various intermittent problems like performance degradation, quality degradation can be avoided thus resulting in high test quality. Also the fault coverage is high in the case of SBST.
In [1], [2] and [3] the authors suggested methodologies based on Instruction Set Architecture (ISA).. In [4], the authors proposed structural component-oriented approach. In [5] the authors proposed specific self test routines based on loop of instructions.Online SBST can be used improve the relaibilty of the system.For that many Optimization techniques have been proposed.

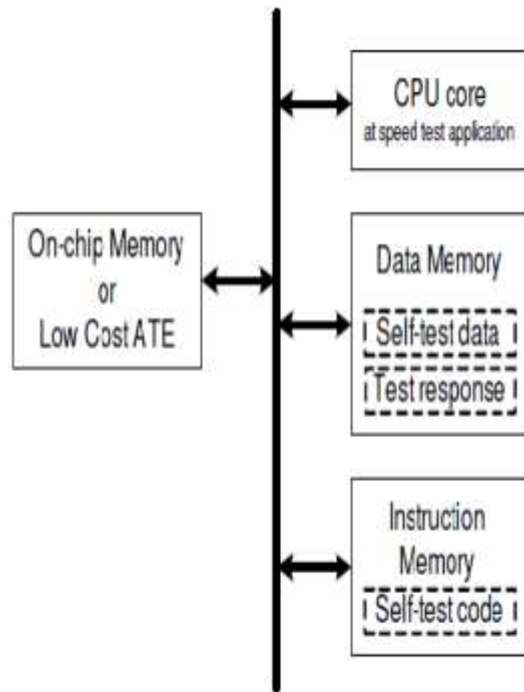

Figure 2: Architecture of SBST

Energy Optimization Methodologies.

Multi ThreadedSBSTgenerates an efficient multithreaded version of the test program and schedules the resulting test threads into the hardware threads of the processor to reduce the overall test execution time and on the same time to increase the overall fault coverage.In other scheme least amount of CPU cycles are taken and operands are selected based on hamming distance.Here it is assumed that the SBST routines are not available at the memory.[10] Various SBST routines are available to test the validity of the sensed data.But the various cases considered are

1) The SBST routines are located in a specific position in the flash memory of the WSN node and therefore routines cannot be updated and thus downloading is irrelevant.

2) The WSN node has some free space in its flash memory where the SBST routines reside. The routines can be updated a number of times during the lifetime of the application. The new routines should also fit in the available space in the flash memory. The number of updates is considerably smaller than the number of executions of the routines.

3) The WSN node does not have any space in the flash memory and every time the routines are executed they are downloaded from a relay node.

4. Conclusion

WSN are used in many geographical area to monitor temperature pressure,humidityetc.Battery power is an very important factor of WSN.ATE, BIST, SBST methods can be used to check the reliability and the accuracy of the system. Among them, the SBST methods are the most reliable. The SBST routines may be initially available in the flash memory.They can also be downloaded.SBST also uses the energy in an optimized fashion hence its very efficient.

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